WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:
a substrate;
a first gate of an N-channel transistor over the substrate;
a second gate of a P-channel transistor over the substrate;
a first spacer insulating region adjacent to the first gate having a first width at its base;
a second spacer insulating region adjacent to the second gate having a second width at its base, the second width is greater than the first width.

2. The integrated circuit of claim 1 wherein:
the first spacer insulating region includes a first number of sidewall spacers;
the second spacer insulating region includes a second number of sidewall spacers, the second number is greater than the first number by at least one.

3. The integrated circuit of claim 2 wherein the second number is greater than the first number by one.

4. The integrated circuit of claim 1 wherein:
the first spacer insulating region includes a first number of sidewall spacers having a width at its base of 200 angstroms or greater;
the second spacer insulating region includes a second number of sidewall spacers having a width at its base of 200 angstroms or greater, the second number is greater than the first number by at least one.

5. The integrated circuit of claim 1 wherein:
the first spacer insulating region includes a first number of liners;
the second spacer insulating region includes a second number of liners, the second number is greater than the first number by at least one.

6. The integrated circuit of claim 1, further comprising:

a first channel region under the first gate; and

a second channel region under the second gate;

wherein:

the first spacer insulating region adds a first incremental compressive stress to the first channel region; and

the second spacer insulating region adds a second incremental compressive stress to the second channel region, wherein the second incremental compressive stress is greater than the first incremental compressive stress.

7. The integrated circuit of claim 1 wherein the substrate is characterized as having silicon on an insulator configuration.

8. The integrated circuit of claim 1 wherein the first spacer insulating region and the second spacer insulating region each include a sidewall spacer including nitride.

9. An integrated circuit, comprising:

a substrate;

a first gate of an N-channel transistor over the substrate;

a second gate of a P-channel transistor over the substrate;

a first silicide region in the substrate for the N-channel transistor, wherein the first silicide region is a first distance from the first gate; and

a second silicide region in the substrate for the P-channel transistor, wherein the second silicide region is a second distance from the second gate, wherein the second distance is greater than the first distance.

10. The integrated circuit of claim 9, further comprising:

a first channel region under the first gate having a first stress; and

a second channel region under the second gate having a second stress that is relatively less tensile than the first stress.

11. The integrated circuit of claim 10, wherein:
the first silicide region and the second silicide region exert a tensile stress.

12. The integrated circuit of claim 9, further comprising:
a first channel region under the first gate; and
a second channel region under the second gate;
wherein:
the first silicide region adds an first incremental tensile stress to the first channel region; and
the second silicide region adds a second incremental tensile stress to the second channel region, wherein the second incremental tensile stress is less than the first incremental tensile stress.

13. The integrated circuit of claim 9, further comprising:
a first channel region under the first gate; and
a second channel region under the second gate;
a first spacer insulating region above the substrate and between the first gate and the first silicide region; and
a second spacer insulating region above the substrate and between the second gate and the second silicide region;
wherein:
the first spacer insulating region adds a first incremental compressive stress to the first channel region; and
the second spacer insulating region adds a second incremental compressive stress to the second channel region, wherein the second incremental compressive stress is greater than the first incremental compressive stress.

14. The integrated circuit of claim 9, further comprising:

a first channel region under the first gate;

a second channel region under the second gate;

a first pair of extension regions in the substrate adjoining the first channel region; and

a second pair of extension regions in the substrate adjoining the second channel region.

15. The integrated circuit of claim 9, further comprising:

a first spacer insulating region above the substrate and between the first gate and the first silicide region having not more than one sidewall spacer having a width at its base of 200 angstroms or greater; and

a second spacer insulating region above the substrate and between the second gate and the second silicide region comprising two sidewall spacers having a width at its base of 200 angstroms or greater.

16. The integrated circuit of claim 9, further comprising:

a first spacer insulating region above the substrate and between the first gate and the first silicide region including a first number of spacers; and

a second spacer insulating region above the substrate and between the second gate and the second silicide region including a second number of spacers, wherein the second number is greater than the first number by at least one.

17. The integrated circuit of claim 9 wherein the substrate is characterized as having a silicon on an insulator configuration.

18. A method comprising:

providing a substrate;

forming, over the substrate, a first gate for an N-channel transistor and a second gate for a P-channel transistor;

forming a first sidewall spacer for the N-channel transistor lateral to the first gate and a second sidewall spacer for the P-channel transistor lateral to the second gate;

forming a third sidewall spacer for the N-channel transistor lateral to the first sidewall spacer and a fourth sidewall spacer for the P-channel transistor lateral to the second sidewall spacer;

providing a first mask over the first gate;

implanting dopants, while the first mask is over the first gate, of a first conductivity type into the substrate;

removing the first mask after the implanting the dopants of the first conductivity type;

providing a second mask over the second gate;

implanting dopants, while the second mask is over the second gate, of a second conductivity type into the substrate; and

removing the third sidewall spacer while the second mask is over the second gate.

19. The method of claim 18, further comprising:

forming a first liner over the first gate and a second liner over the second gate prior to the forming the first sidewall spacer and the second sidewall spacer; and

forming a third liner over the first sidewall spacer and a fourth liner over the second sidewall spacer prior to the forming the third sidewall spacer and the fourth sidewall spacer.

20. The method of claim 19 wherein:

the third liner is of a first material;

the third sidewall spacer is of a second material that is selectably etchable from the first material.

21. The method of claim 20 wherein the first material includes an oxide and the second material includes a nitride.

22. The method of claim 18, further comprising:

forming a first silicide region in the substrate for the N-channel transistor, wherein the first silicide region is a first distance from the first gate; and

forming a second silicide region in the substrate for the P-channel transistor, wherein the second silicide region is a second distance from the second gate, wherein the second distance is greater than the first distance.

23. The method of claim 18, wherein the providing the first mask occurs prior to the providing the second mask.

24. The method of claim 18, wherein the providing the first mask occurs after the providing the second mask.

25. The method of claim 18 further comprising:

implanting dopants in a first region and a second region of the substrate of the second conductivity type for forming a first extension and a second extension for the N-channel transistor, respectively; and

implanting dopants in a third region and a fourth region of the substrate of the first conductivity type for forming a third extension and a fourth extension for the P-channel transistor, respectively.

26. The method of claim 25, wherein:

the implanting dopants in the substrate of the second conductivity type are utilized to form a first doped region and a second region in the substrate that are in contact with the first extension and second extension, respectively; and

the implanting dopants of the first conductivity type are utilized to form a third doped region and a fourth doped region in the substrate in contact with the third extension and the fourth extension, respectively.

27. The method of claim 18, further comprising:

implanting dopants, while the second mask is over the second gate and after removing the third sidewall spacer, of the second conductivity type into the substrate.

28. The method of claim 18, wherein the first gate comprises polysilicon.

29. The method of claim 18, wherein the first gate comprises a metal.

30. The method of claim 18 wherein the substrate is characterized as having a silicon on an insulator configuration.

31. The method of claim 18 wherein:

the forming the first side wall spacer and the second sidewall spacer further includes depositing a first layer of spacer material over the substrate and etching the first layer with a dry etch;

the forming the third side wall spacer and the fourth sidewall spacer further includes depositing a second layer of spacer material over the substrate and etching the second layer with a dry etch;

32. The method of claim 27 wherein the first layer and the second layer include nitride.

33. The method of claim 18, further comprising:

forming a first silicide region in the substrate for the N-channel transistor, wherein the first silicide region is substantially aligned with the first sidewall spacer; and

forming a second silicide region in the substrate for the P-channel transistor, wherein the first silicide region is substantially aligned with the fourth sidewall spacer.